echo

DIGITAL VOICE STORAGE RETRIEVAL UNIT

MANUAL

telos systems

Telos Systems ECHO VOICE STORAGE/RETRIEVAL SYSTEM

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Introduction

The Echo is the second product from a very small company, Telos Systems. As with the Telos 10 digital hybrid system, the Echo was designed to solve a problem which I have encountered in my own work as a radio station engineer.

Unhappily, I had been using cart machines for an application for which they are ill-suited: playing recorded messages to listeners on the phone. Cartridges are OK for on-air playback, but are frequently unreliable (to say the least!) when they are called upon to serve the continuous playback demands of concert lines, weather lines, ski information lines and the like.

At my station, our concert line gets as many as 1,000 calls a day! The has-been cart machines we were using were a constant source of frustration. Broken tapes, worn heads and bad pinch rollers often resulted in listener complaints, angry program directors, and unhappy engineers.

Technology to the rescue!

Recent advances in digital speech companding technology, combined with rapidly falling RAM memory cost has made possible a nifty solution to the problem of answering the phone reliably: record and play the message from solid-state memory IC's, not from unreliable mechanical contraptions.
The Echo uses 1 Mbyte of dynamic ram memory controlled by a Z80 processor. A special signal processing IC allows 4 minutes of telephone-grade speech to be stored.

A built-in phone line answering circuit allows simple no-hassle installation: merely provide AC power, and connect the phone line.

Operation is simple too. The control layout is designed to simulate a simple cassette machine. Functions are labeled so that anyone familiar with analog tape machines can intuitively figure-out what to do without resorting to a manual or learning complicated control sequences.

Introduction (cont)

In addition there are a few neat features to wow jaded GM's and PD's. An LED display counts seconds in the record mode and number of calls received in the auto-answer/play mode. A front panel speaker makes checking messages easy. Full remote control facilities allow messages to be recorded in the production studio.

There are a few features engineers will like, too. A front panel XLR-type balanced mike input, along with a balanced line-level input on the rear panel. A battery back-up scheme and a special circuit called a "watchdog timer" that prevents problems from power glitches and failures. An effective AGC to prevent record level problems. Solid, conservative design and construction. Built-in diagnostics. Complete component-level troubleshooting information, or a board-swap repair program your choice. A quality PC board with all component legends screened clearly. Easy access to all parts.

The goal of Telos Systems is to provide high-quality, creative and cost-effective solutions to broadcast problems. And, of course, a few bucks to the owner, ME! So far, so good.

As always, keep on keepin' the GM happy...

- Steve Church

A note about Service

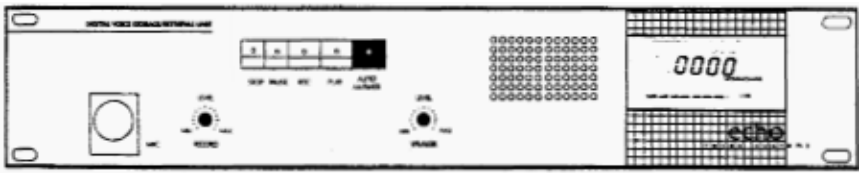
Telos Systems is a small company. I'm committed to provide the advantages of small company service to you.
A very few service-oriented dealers have been enlisted to be your front-line contact in the event you should need questions answered or help of any kind. This allows me to continue in my primary role as a working-stiff CE, while at the same time ensuring that you get what you need when you need it.

Echo dealers have been instructed, however, to have you contact me directly in the event that they are unable to solve your problem quickly.

This strategy has been successful with Telos 10 owners. In almost every case where a part or a board-swap was required in order to solve a problem, the part or board was shipped within one day. It is my goal to have no defects, of course - but if you have an Echo malfunction, you can count on a quick solution.

Operation

The Echo was designed to be easily understood and operated by anybody who knows how to use a simple cassette recorder. Use of the Echo should be intuitive, for the most part. However, there are a few interesting features/quirks that may not be immediately apparent.



Since you've got to record before you play, let's discuss that first.

RECORDING - In order to record, you'll have to connect either a microphone to the front panel XLR input or a line—level source to the rear-panel phone jack. See the installation section for details.

Adjust the record level control so that the led level display is indicating normally. This is not critical since the internal automatic gain control will take care of all but the most extreme input levels.

Press the RECORD button and talk. The SECONDS/COUNTER display will indicate elapsed time. The maximum time is *256* seconds.

When you've finished your message, press the STOP button. This terminates recording and causes an ending "marker" to be placed at the end of your message. During recording, you may pause by pressing the PAUSE button. You are then able to resume recording by pressing the RECORD button again.

PLAYING back - Press the PLAY button and adjust the speaker level control for the desired volume.

You can use the PAUSE button in the play mode just as you would expect. In fact, one potentially useful feature is that you can go into the record mode after pausing during playback. This allows you to extend an already recorded message or to change an existing “tag.”

AUTO ANSWER/PLAY mode -This is the mode which is used to answer incoming phone calls. To establish the auto answer mode, press the white AUTO ANSWER button. As calls come in, they are answered by the ECHO and the LED counter counts the number of calls (up to 9999, then starts over again at 0000). The bar graph indicates the presence of audio.

Loss of AC power can result in a meaningless call-count display. Pressing the stop button will reset the counter to zero.

If the PLAY button is pressed when in the auto answer mode, the message will be played-back continuously. Since the Echo is likely to be used for long periods of time without attention in the auto answer mode, it incorporates a special feature called a “watchdog timer” to ensure that power line failures and “glitches” don’t cause the unit to malfunction.

If there is a power failure, the battery will maintain the message in memory for approximately one hour. When power is restored, the Echo will automatically go into the auto answer mode.

Power line glitches can also cause the unit to go into the auto answer mode. No loss of memory will occur.

If erratic operation is observed, a manual reset may be required. This is accomplished by pressing the AUTO button.

Selecting number of plays in the Auto Answer mode

The number of times the message is played to callers is selectable using an internal “dip switch.”

The unit is shipped with the switch set for single play operation. If you need to select two or three plays, you will need to remove the top cover to get access to the dip switch.

With the cover removed, locate the dip switch, and turn on only the switch corresponding to the number of plays you desire.

This dip switch is also used to access internal test diagnostics described later.

CAUTION: With the top removed, there is 110V AC present near the left rear of the unit (by the fuse and power connector, and also the white plug that mates with J2). If you are unsure of where the AC is present, PULL THE PLUG BEFORE YOU MUCK ABOUT WITH THE INTERNALS OF THE ECHO!

About the Battery and the Battery Switch

The Gel-Cell-type battery used in the Echo may have to be replaced after three to four years of service, according to the manufacturer.

It’s probably a good idea to check the battery every now and again by pulling the AC cord to see how long the message is retained in memory.

The rear panel battery switch is provided to keep the battery from being fully discharged when the unit is expected to be unplugged for a long period of time (over an hour). When you expect to have it unplugged, turn the battery switch to the off position.

The Echo is shipped with the battery charged and the switch off.

Installation

Echo installation is very simple.

1) Apply AC.

2) Turn the battery switch (on the rear panel) to the on position. If the battery has been allowed to fully discharge, it may be a few moments for all of the Echo functions to become operational. In addition, if memory contents have been lost because of battery discharge, pressing the play button will yield a solid tone at very high level. Doing this while drinking coffee is not recommended.

3) Plug the phone line into the modular phone connector on the rear panel.

4) Plug a microphone into the front panel XLR connector, or a line level input into the rear panel 1/4” phone jack.

The rear panel line input is balanced and uses a tip-ring--sleeve “stereo” type 1/4” jack.

For balanced sources, the two hot leads go to tip and ring and the shield goes to the sleeve.

For unbalanced sources, use a “mono-type” plug, or short the sleeve to the ring of a tip-ring-sleeve type plug. The hot audio lead would then go to the tip, of course, while the shield would go to the sleeve.

If you need to use any of the remote control functions, move ahead to the next page.

Remote Control

The front panel switches and the indicator LEDS are remotable via the rear panel DB25 25-pin connector. A balanced audio output is also available on this connector.

As described earlier, a separate 1/4” phone jack is provided for line level input. The mic and line inputs are simultaneously active.

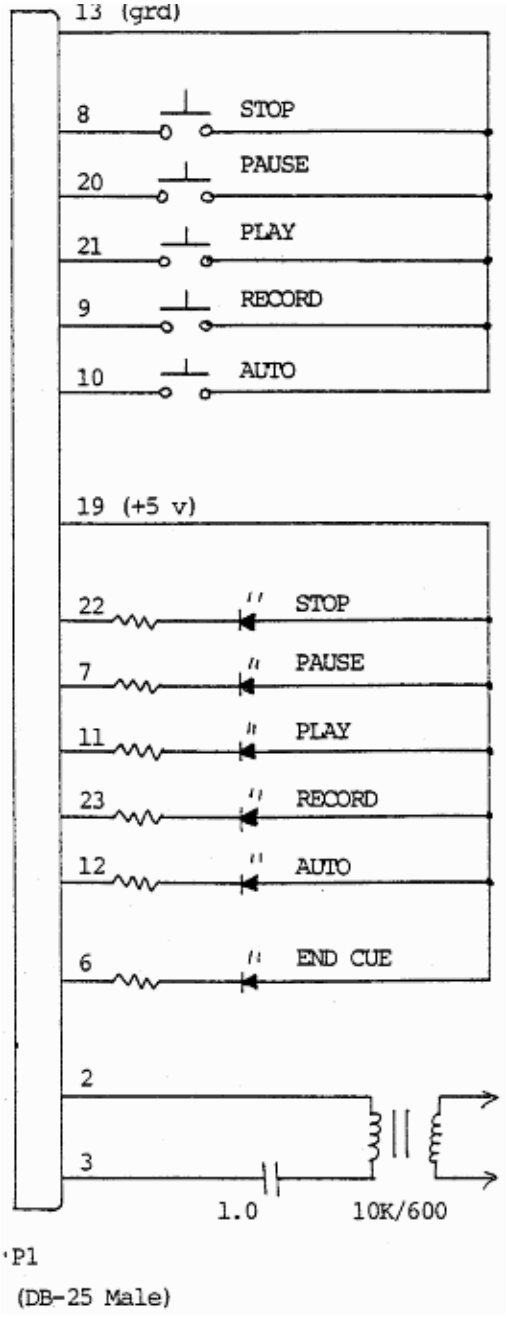
The audio output level is approximately -10 dBm.

The remote inputs connect between the ground pin and the appropriate input function pins. They are thus pulling a high voltage (5v) to ground. The internal pull-up resistor is 1K. The inputs are well buffered and debounced, so there should be no problem with long cable runs.
The outputs are pulled to ground when active. Thus your external indicators should connect between the +5v pin and the appropriate output pin. YOU MUST PROVIDE THE REQUIRED CURRENT-LIMITING RESISTORS IF YOU USE LEDS AS YOUR REMOTE INDICATORS. Usually, 330 ohms is the value used (for 15 ma LED current).

Remote Connector Pin-out:

Function	Pin	
STOP switch	8	
PAUSE switch	20	
PLAY switch	21	
RECORD switch	*9*	
AUTO switch	10	
Ground (switch common)	1	
STOP indicator	22	
PAUSE indicator	7	
PLAY indicator	11	
RECORD indicator	*23*	
AUTO indicator	12	
+5v (indicator common)	*2*	
Audio out +	(see next page)	
Audio out -		
Phone line	24	
Phone line	25	
End Cue output	6	(closure to ground)

Remote Control Example Schematic



Note:

Audio output at pins 2 & 3 are transformer balanced. When the Echo is answering a call, this output is connected to the phone line. The capacitor and transformer indicated are required to isolate user equipment if it is expected that a call might be answered while this output is connected.

Circuit Description & Troubleshooting

Introduction

The Echo circuitry is made up of analog and digital sections. The analog audio processing and output sections should present no problem to the experienced troubleshooter. Finding problems should be as simple as tracing with an oscilloscope to find where in the circuit the signal quits or becomes distorted or whatever.

The digital section has as it's central element the very common Z80 microprocessor. While a "textbook simple" approach has been taken toward the design of this portion of the Echo, some tricky troubleshooting may be required to nail down problems, particularly if the timing circuits or dynamic ram interface section is involved.

If you are unfamiliar with microprocessors, and wish to learn, a good tutorial discussion of Z80-based circuits is given in BUILD YOUR OWN Z80 COMPUTER, Steve Ciarcia, Byte Books. This book is often found at local bookstores, or may be ordered by them.

Diagnostic routines are included to help you find certain kinds of problems. Since these are very simple to use, they are always a good first step. The next manual section describes the use of these routines.

While full component-level troubleshooting information is included here, keep in mind that a board swap repair program is available on all Telos products, if you prefer not to tackle nitty-gritty troubleshooting yourself. Please contact your dealer for particulars.

Circuit Description and Troubleshooting Diagnostics

There are two diagnostic routines, which are normally used during production testing which may be useful if you suspect problems with the microprocessor or memory sections of the echo. One tests the basic functioning of the Z80 processor and the input/output circuits; the other is used to test the memory array and pinpoint bad memory chips.

THE I/O TEST DIAGNOSTIC MODE -

This diagnostic mode is used to confirm the proper operation of the core microprocessor circuit and the input/output sections.

The test is entered by turning dip switch #[1]s 2 and *3* ON with #1 off (open) and then causing a reset by pressing the AUTO button. The AUTO button led will illuminate. Each button will light it's associated led as long as it is pressed. The AUTO button will pull-in the line relay.

THE MEMORY TEST DIAGNOSTIC MODE -

This mode is entered by turning all 3 of the dip switches on (opposite "open") and then performing a reset by pressing the AUTO button.

The STOP LED will flash. To begin the test, press the STOP button. The counter will begin counting and the STOP LED will be on solid.

A successful completion of the test will result in the counter indicating 256, and the STOP led will flash again.

If there is a memory error, all of the LEDS will flash and the line relay will cycle. The counter indicates the bad memory column as follows:

0-63	column0 (U2-9)
64-127	column1 (U10-17)
128-191	column2 (U18-25)
192-255	column3 (U26-33)

Diagnostics (cont)

Pressing the STOP button again will isolate the row position of the bad IC within the column previously indicated. A 0 count corresponds to the memory IC nearest the rear panel, while a 7 count would indicate that the IC nearest the front is bad.

When pressing the STOP button, hold it down long enough only to start the test process. Otherwise, some counts may be lost, and you may be misled as to the location of the faulty IC.

Circuit Description and Troubleshooting
Board removal

The main board is removed by:

1) Unscrewing the 1/4” phone jack retaining nut,

2) Unscrewing the 2 screws that hold the DB- 25 multi-pin remote connector to the rear panel,

3) Unscrewing the 3 retaining screws accessible from the top,

4) Unscrewing the 2 screws securing the spacers near the power transformer FROM THE BOTTOM OF THE CASE (the transformer obstructs access to the screws from the top). Of course, if you have a screwdriver with a small enough shaft, there is no reason you couldn’t remove the screws from the top.

SPECIAL NOTE: The power supply regulators must have a heat sink in order to operate properly. This means that you should have the two regulator mounting screws in place while the Echo is powered-up. No permanent damage will occur if you forget to do this, but there will be very flaky problems as the regulators heat-up and then shut-down as they are supposed to.

Circuit Description and Troubleshooting

Circuit discussion - digital section

All digital signals are TTL compatible levels which means that a high signal would be 2.4v or above, and a low would be under .8v.

The central circuit element is the Z80 microprocessor. The Z80 moves the digitized audio from the signal processor to and from the appropriate memory locations and provides all of the control functions by responding to the pushbutton and other inputs. With the exception of the dynamic ram circuits, the approach used in the echo is “textbook simple.”

The Z80 (U1) executes the machine-level software programmed into the 2716 EPROM (U43). U43 puts it’s data on the bus when it’s EPCS pin goes active. The EPROM is selected when address line A15 is low; that is when the Z80 is requesting data from locations hex 0000 to 7FFF. Sections of U46 and U47 provide the required gating to ensure the EPROM is selected only when A15 is low MRQ is active.

U40 is a buffer. It provides the required drive to the data bus from the Z80. It also buffers the Z80 input, as well. The Z80 RD output causes U40’s direction of operation to be appropriate.

There is one input IO port, U39. It puts the input data on the bus when it’s select line, IOSEL3 becomes active. U53 and U54 are special buffer ICs, which are intended for use with long input lines (they’re actually intended for use with computer serial RS- 232 inputs); thus, they have provision for rejecting spurious inputs. The capacitors, C23-26 slow input response for this purpose.

There are two output ports, U42 and U41. U42 is used to drive the indicator LEDS, the END CUE output, and the line relay. U41 is the bank select port for the memory section and drives the AUTO indicator and the front panel LED counter COUNT line. Both of these pick up and latch data from the bus when their IOSEL lines go active.

The IOSEL signals are generated by one section of U34, which decodes the lower two address lines to four outputs.

The signal processor, a special programmed NEC 7730 IC (U58), operates as a peripheral to the Z80. It is, in effect, both an input and an output port. This is where the Z80 sends the digitized audio data during play, and where it gets it during record.

U57 is a special type of Analog-to-Digital and Digital-to-Analog converter called a CODEC. Useful for telephone-grade audio, it contains built-in input and output filters. It connects directly to the signal processor via two serial lines, SI and SO.

The circuit elements in the upper right corner of the schematic are the clock generator. It generates synced clock outputs for the 7730, the Z80, and the CODEC. The 7730 gets 8 MHz, the Z80 gets 4 kHz, and the CODEC gets 2 kHz plus a special frame-sync signal. See the clock timing chart for output waveforms.

The most difficult part of the Echo to understand is the dynamic memory section. The Echo has 1 megabyte of memory. Each DRAM chip has a capacity of 256K bits. Each byte needs 8 chips, since each chip is only one bit “wide”, to use the usual computer terminology. Thus, the memory bank consists of 4 rows of 8 chips to make up the 1 Meg by 8-bit memory array.

The 4 rows are accessed in order during the 4-minute play/record time, with the first row storing the first minute; the second row the second minute, etc.

Since the Z80 cannot directly address 1 Mbyte of memory, a bank select scheme is used to extend the system addressing range. When it’s time to switch to the next bank, the new bank value is output to the U41 output port. We’re using 15 address lines from the Z80 directly for the address Isb’s (A0-A14), and 5 from the bank select port for 20 total address bits. This is the required number of bits to address 1 Mbyte. BS1 and BS2 are decoded by one-half of U34 to select from the 4 DRAM rows.

Dynamic memory is the lowest-cost and least space/energy consuming way to get lots of storage capacity. It is certainly the only practical way, at present, to get enough capacity cheaply for applications like the Echo.

There are disadvantages to using DRAM’s which must be dealt with, however. Since DRAM’s store information as a charge on a capacitor, the memory must remain powered and “refreshed” by the Z80 software regularly in order to retain data. The battery is used to ensure that power interruptions don’t cause the message to be erased. A watchdog timer, discussed later, makes sure the Z80 is always running so that it can perform it’s refresh function.

The second DRAM disadvantage is the complexity of the interface circuit. In order to keep the memory IC packages small, the number of pins are limited and the address inputs are “multiplexed.” That is, the 18 required address inputs are shared on only 9 pins. Internal latches retain the 9 bit values in order that the full 18 bits are available at once to select the appropriate memory cell. Two inputs, RAS (Row Address Strobe) and CAS (Column Address Strobe) are used to latch in the appropriate address bits at the right time. The address multiplexing and the control of the CAS and RAS strobes are accomplished using a number of the remaining IC’s.

There are few things in the known universe as terrifying as the timing requirements of DRAM's! Take a look at the timing diagram (in the appendix) for an idea of what's involved. Fortunately for you, the circuit is already designed - you just have to fix it. Remember, it did work once - so, it certainly can again!

First, let's examine what happens in the record mode. You will need to refer to the memory timing chart and the schematic in order to make sense of this discussion.

The memory write cycle is begun when MRQ (Memory ReQuest) goes active out of the Z80. U46 (12,13,11) gates MRQ with RFSH so that GATED MRQ is only active during non-refresh cycles. Since the refreshing is handled by software reads, the Z80 hardware refresh cycle is ignored. GATED MRQ becomes the RAS (Row Address Select) for the DRAMS. That means that the row addresses are latched in to the RAM chips. The three multiplexers (U35-37) are sending the low 9 address bits through to the DRAM'S at this time.

Also, note that GATED MRQ is combined with RD in such a way that the DRAM WE (Write Enable) becomes active at the same time as MRQ. This allows data to be written into the memory.

GATED MRQ also goes to the D input of flip-flop U44. This causes MUX to go active (low) on the next rising edge of the Z8O clock, in order to provide the required delay between RAS being applied to the DRAMS and the multiplexers switch to the column addresses, which is controlled by MUX.

So far, we have the row address bits latched in to the DRAMS, and we've just switched the multiplexers so that the column data is presented to the address inputs. All that remains is to latch the column data in.

That happens when DMUX (Delayed MUX) goes active and enables U34 to output the appropriate CAS signal. DMUX is gated with A15 to ensure that the Z80 is calling upon the DRAM's and not the EPROM memory. Remember that A15 must be high to allow access of the DRAM memory. Notice that DMUX does not become active until after the column addresses are presented to the memory chips, since DMUX is actually an output from one of the multiplexers (U37). Proper delay time is ensured by the CAS signal only being generated after two additional gate delays caused by U46 (9,10,8) an U34.

U38 is a buffer to provide drive to the DRAM bank. The multiplexers (U35-37) are also buffers. The resistors help to control ringing and overshoot.

As your reward for reading through that discussion on the DRAM circuits, we'll now address the line answering section. It's much easier! The NE2 neon bulb couples the AC ring voltage thru to the opto-isolator (U56). R46 is the current limiting resistor, and D19 prevents U56 from being blown-out from reverse potentials. When a ring comes in, the opto-isolator turns on and the INT signal goes low. INT goes right to the Z80.

The watchdog timer and reset circuit (separate schematic) is made from U70, a dual timer IC, along with the associated components. The software makes sure that IOSEL3 is regularly pulsed low. If this signal stops doing this, the watchdog timer resets the Z80 since it is no longer properly running the program. C71 is a differentiator to ensure that the watchdog only responds to the edge of the pulses. If this were not incorporated, a problem which caused IOSEL3 to be continuously low would not be detected.

When the IOSEL3 signal stops, the first half of U70 times out and causes the second U70 half to output a reset pulse. This output is also fed back to the first timer to force continuous resets until the system starts up. The circuit associated with U47 (11,10) causes a reset upon power-up. Note that this circuit forces a reset upon re-application of AC power even when the battery is turned-on. All of this happens fast enough that the DRAM bank never loses data. In the event that a manual reset is ever needed, the AUTO button is wired to force a reset. The front panel LED count display is generated by the 1CM7217, a full counter display controller. It takes the count input from the U41 IO port, and the counter reset from the STOP button.

Circuit Description and Troubleshooting
Audio circuit discussion

The audio circuitry is straightforward. The mic input is accepted as balanced by U60 (6,5,7). The line input is padded and applied in parallel with the mic input.

U60 (9,10,8) provides pre-emphasis.

U62 is the VCA (Voltage Controlled Amplifier), which performs the AGC action. D17, 18 rectify the audio to produce the control voltage. C14 is the time-constant capacitor. Attack and release times are controlled by R23 and R24.

A gating function is provided to freeze the gain when there is no audio input. This allows fairly aggressive processing without excessive artifacts (where have we heard that before?). The gating approach is unique. The amplified input audio is sent to both fast and slow rectifier/time constant networks (D14, 15 and associated parts), and the two resulting outputs are compared in an op-amp stage configured as a comparator, U61 (5,6,7). This accomplishes a “floating gate” function, which is relatively insensitive to input level. Thus, no gating threshold control is required, and superior gating action is obtained.

U63 (9,6,8) disconnects C14 when gating is active, thus freezing gain.

U63 (2,1,13 & 10,12,11) are used for meter switching. Either the play or record signals are routed to U61 (8,9,10) for amplification and the following parts, which provide the meter time constant, and on to the bar graph front panel meter module.

U57 is the CODEC IC, discussed earlier, which converts the audio to digital and back again. A balanced output from this IC is sent to the phone line transformer, and one side goes also to the speaker amplifier.

The audio drive to the speaker is provided by U59, a single-IC amplifier.

Circuit Description and Troubleshooting
Power Supply

The power supply generates four outputs: +5 v logic (battery- backed), +5 v logic (no-battery), ÷5 v audio, and -5 v audio.

All but the 5 v battery-backed are simple three-leg regulator circuits. The battery-backed supply parallels the output from the rectifier with the battery. If AC goes away, the battery maintains power. Li prevents line spikes from getting through to the regulator and ultimately the logic and processor circuits.

Since the Echo is designed to be used for long periods of time unattended, a number of steps were taken to ensure proper operation even in the presence of AC power glitches.

- The AC connector is filtered.

- A split-type power transformer is used to reduce inter-winding capacitance.
- The battery prevents sags and momentary drops from causing problems.

- The coil (Li) reduces problems from line spikes.

- A large number of carefully chosen bypass capacitors are placed throughout the PC board.

- The watchdog timer immediately restarts the Z80 if it should stop running properly for any reason.

Voltage regulator U68 and its associated components are not used in some units, depending on battery type.

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Appendix

Timing Charts
Manufacturers Data Sheets

OKI

FEBRUARY 1985

SEMICONDUCTOR

MSM41256AS/RS
262144-BIT DYNAMIC RANDOM ACCESS MEMORY — PAGE MODE

GENERAL DESCRIPTION

The OKI MSM41256 is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41256 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

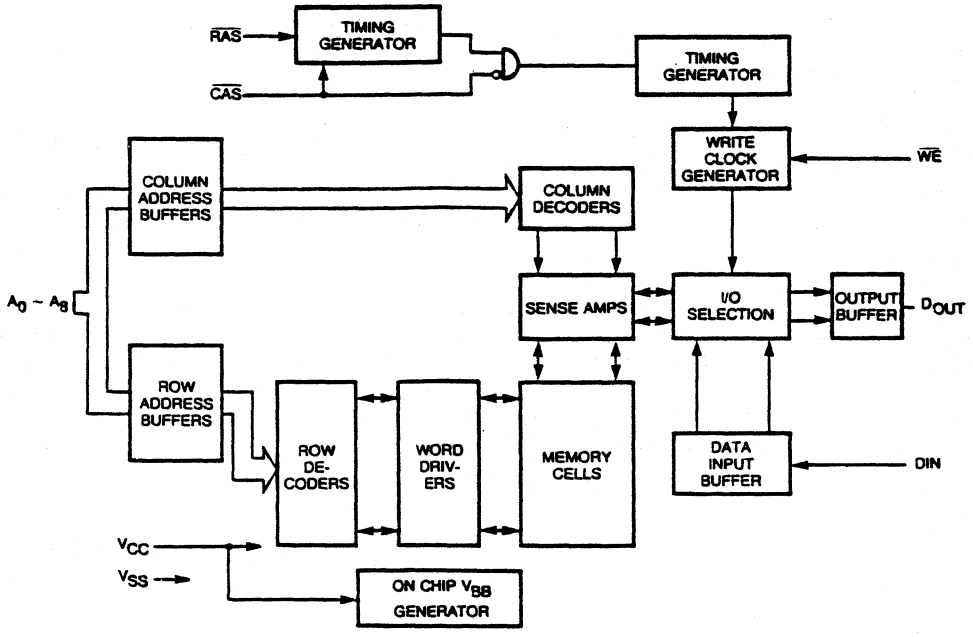
The MSM41256 is fabricated using silicon gate NMOS and OKI's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

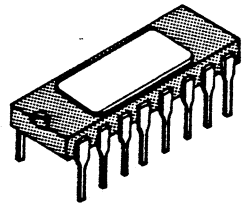
FEATURES

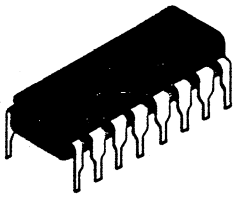
- 262144 × 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150 ns max (MSM41256-15AS/RS)
  200 ns max (MSM41256-20AS/RS)
- Cycle time,
  260 ns min (MSM41256-15AS/RS)
  330 ns min (MSM41256-20AS/RS)
- Low power 385 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 4 ms/256 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance

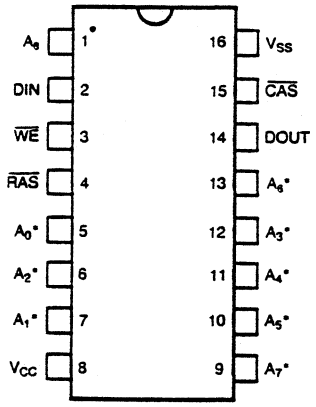
BLOCK DIAGRAM



PIN CONFIGURATION







Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

* Refresh Address

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current	I_{os}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to + 70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		75	mA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		60	mA
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA
INPUT LEAKAGE CURRENT Input leakage current, any input (OV ≤ V_{IN} ≤ 6.5V, all other pins not under test = OV)	I_{LI}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, OV ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	0.4	V V

*Note: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (A_0 ~ A_8, D_{IN})	C_{IN1}	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	pF
Output Capacitance (D_{OUT})	C_{OUT}	7	pF

Note: Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

Parameter	Symbol	Units	MSM41256-15		MSM41256-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4	
Random read or write cycle time	t_{RC}	ns	260		330		
Read-write cycle time	t_{RWC}	ns	325		410		
Page mode cycle time	t_{PC}	ns	145		190		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		75		100	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	75		100		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	75	10,000	100	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	75	30	100	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	20		25		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	45		55		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	120		155		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	0		0		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	120		155		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	60		80		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	60		80		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	120		155		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	75		100		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	150		200		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		25		

NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples: $\overline{RAS}$ only refresh) before proper device operation is achieved.

2) AC measurements assume $t_T = 5$ ns.

3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4) Assumes that $t_{RCD} \leq t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

5) Assumes that $t_{RCD} \leq t_{RCD}$ (max.).

6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geq t_{WCD}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

DESCRIPTION

ADDRESS INPUTS:
A total of eighteen binary input address bits are required to decode any 1 of 262144 storage cell locations within the MSM41256. Nine row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). The nine column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

WRITE ENABLE:
The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

DATA INPUT:
Data is written into the MSM41256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

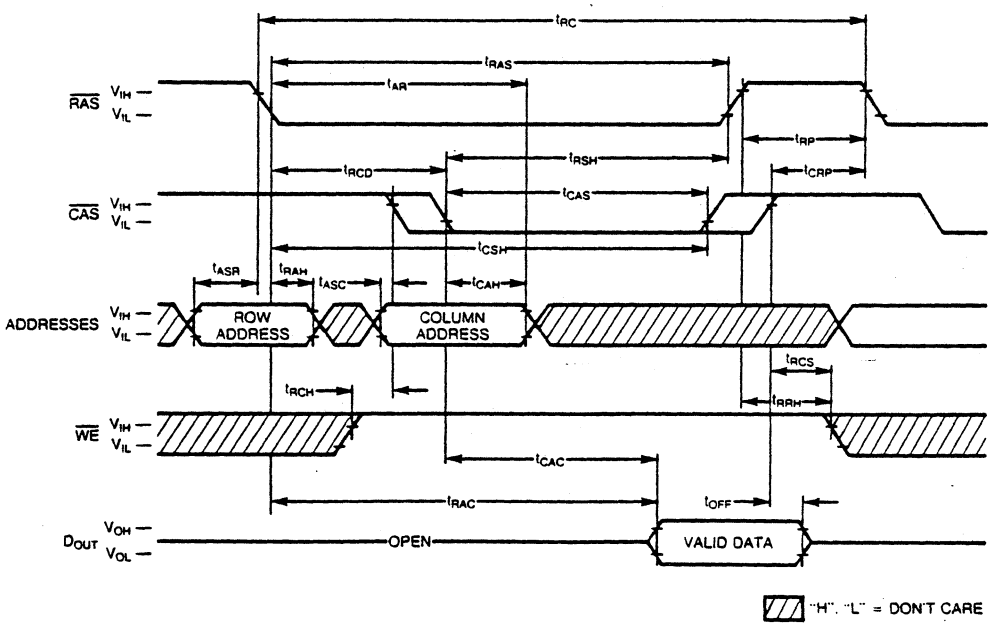
PAGE MODE:
Page-mode operation permits strobing the row-address into the MSM41256 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

REFRESH:
Refresh of the dynamic memory cells is accomplised by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$ at least every four milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

HIDDEN REFRESH:
$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

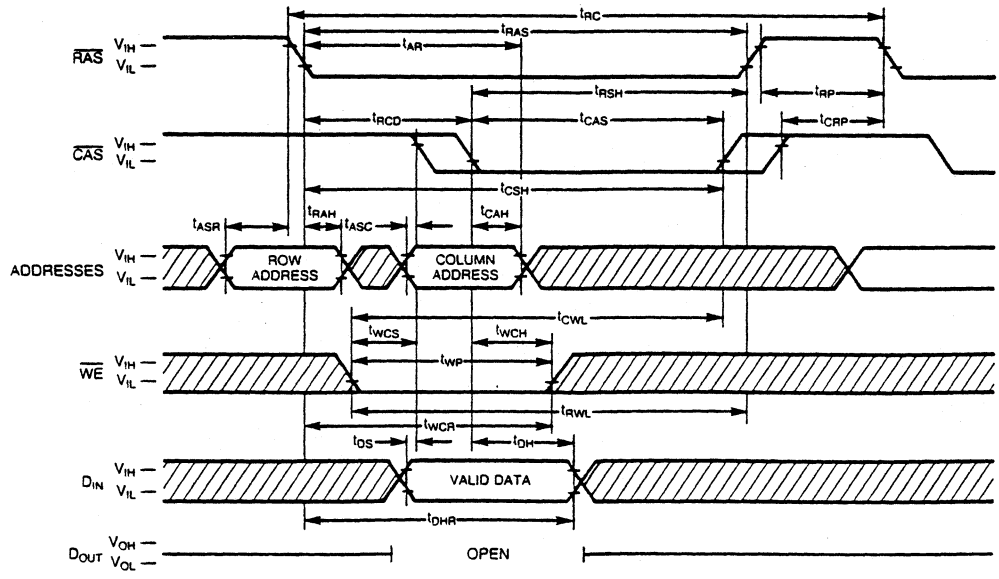
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

READ CYCLE TIMING

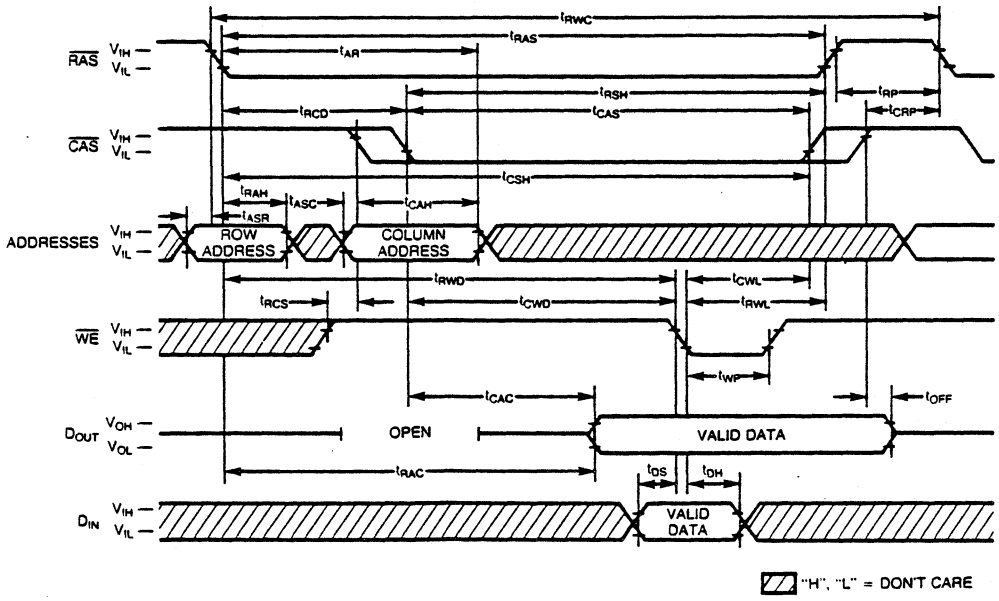


WRITE CYCLE TIMING

(Early Write)

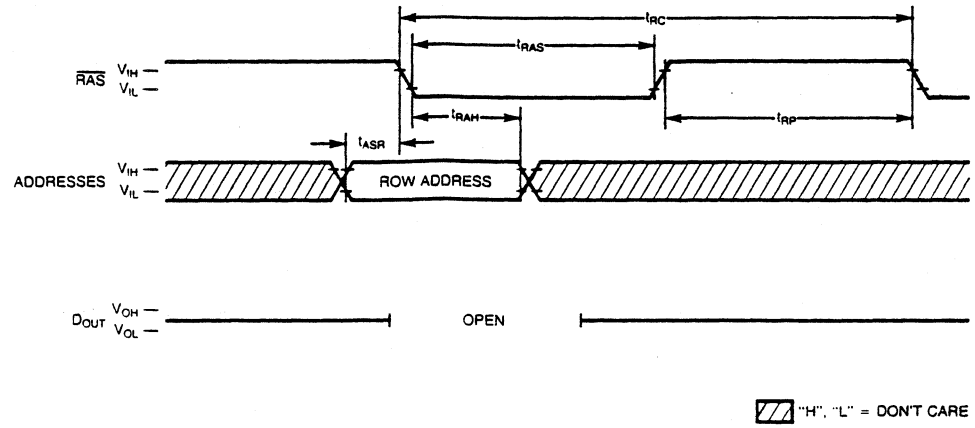


READ-WRITE/READ-MODIFY-WRITE CYCLE

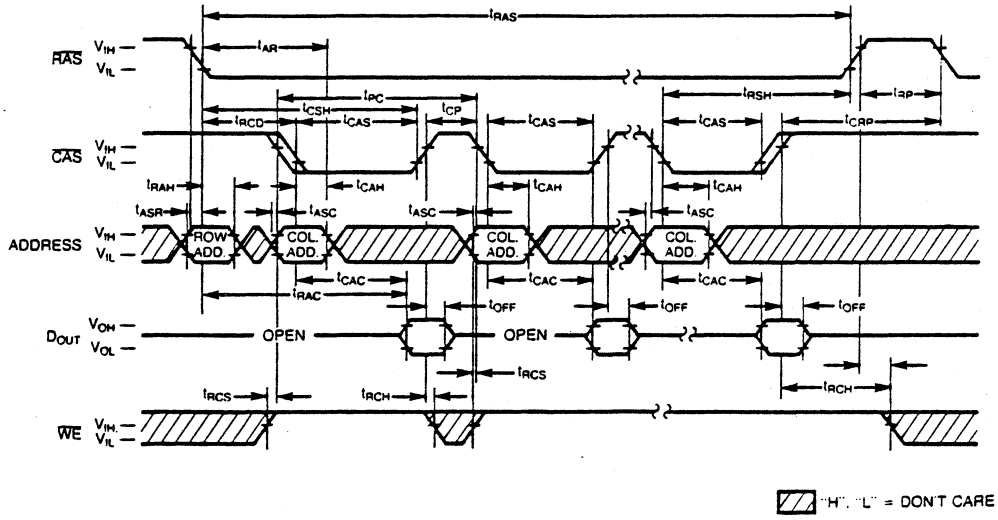


$\overline{RAS}$ ONLY REFRESH TIMING

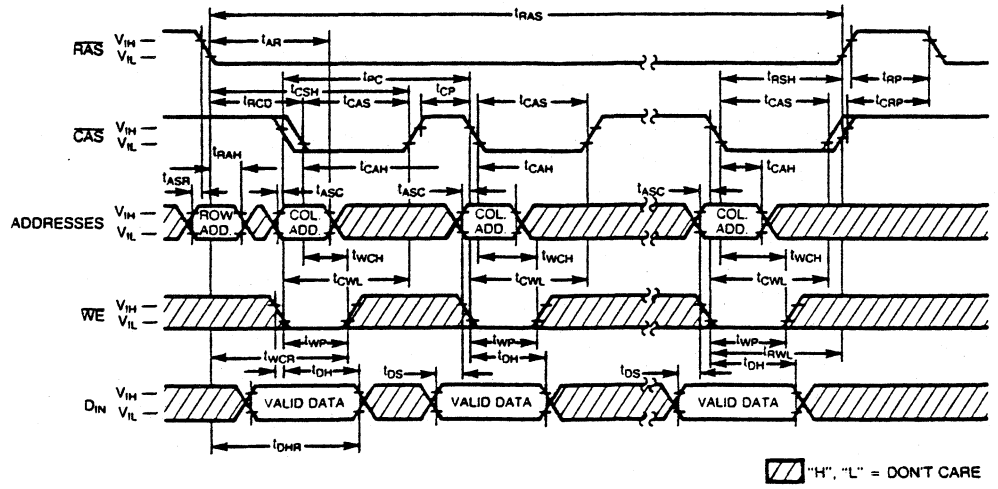
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



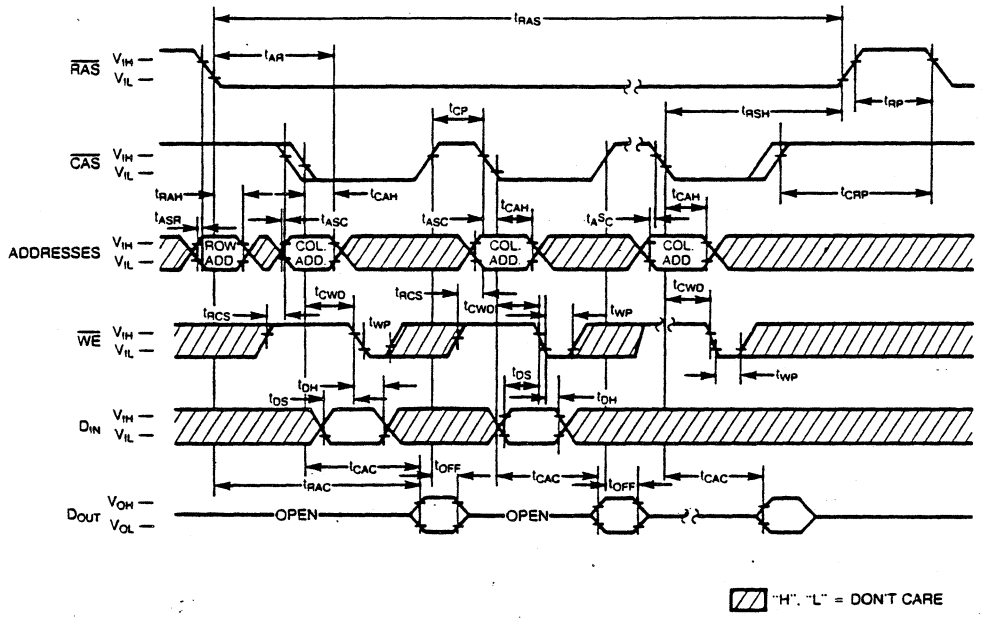
PAGE MODE READ CYCLE



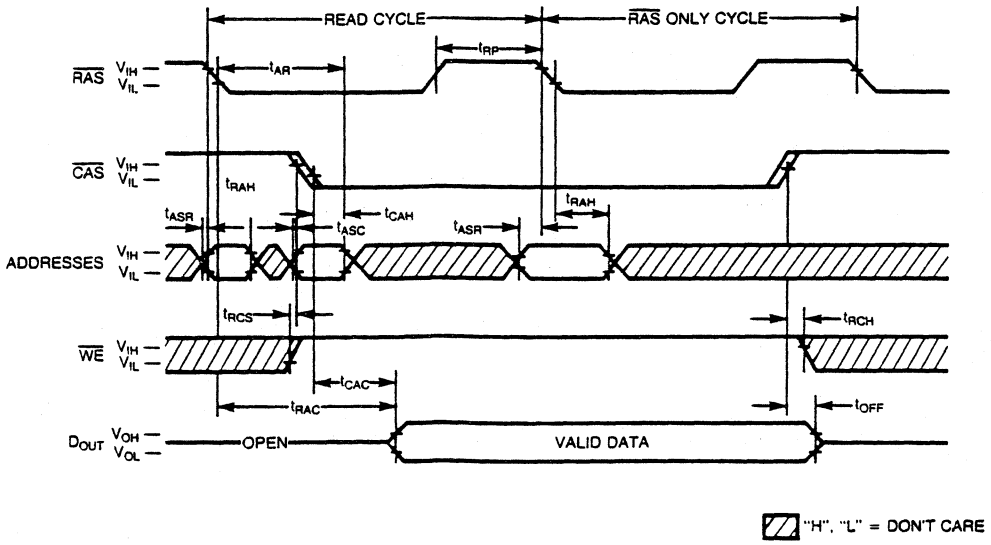
PAGE MODE WRITE CYCLE



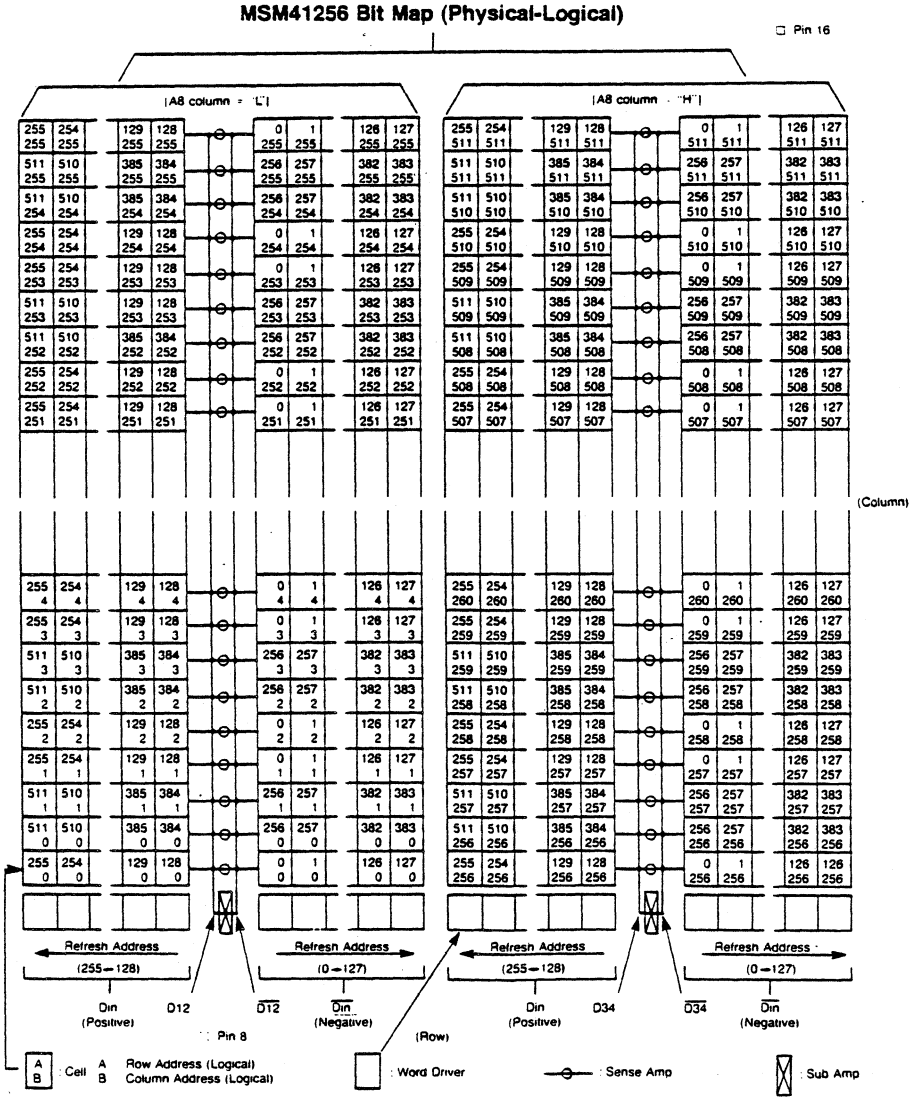
PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRESH



MSM41256 Bit Map (Physical-Logical)



ORDERING INFORMATION

Speed	Package (Note 1)	Pins	Part Number
150 nsec	CDIP	16	MSM 41256-15 AS
	PDIP		MSM 41256-15 RS
200 nsec	CDIP	16	MSM 41256-20 AS
	PDIP		MSM 41256-20 RS

Notes: PDIP = Molded dip
CDIP = Ceramic side-brazed dip

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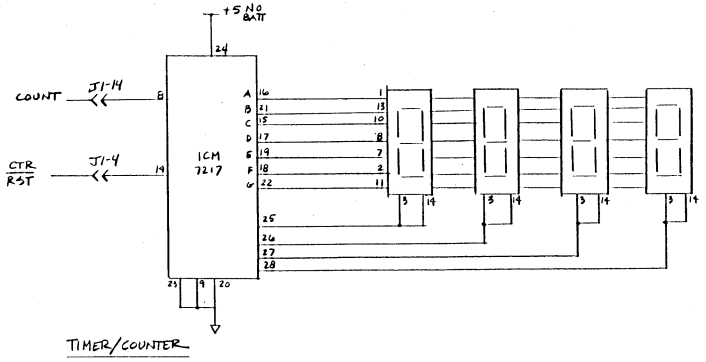
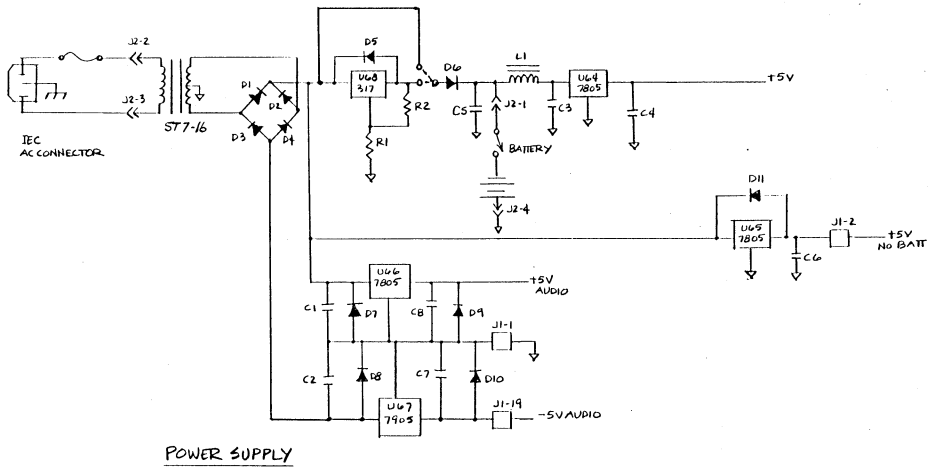
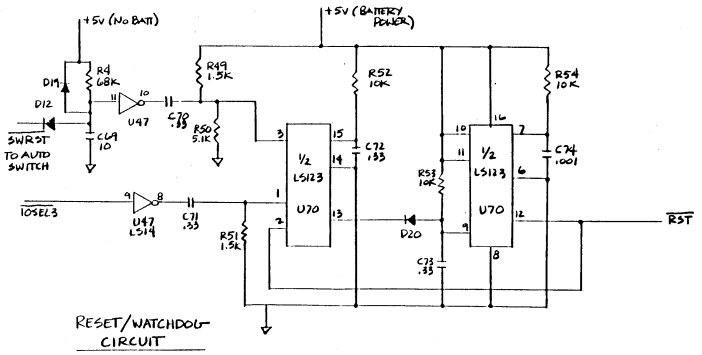
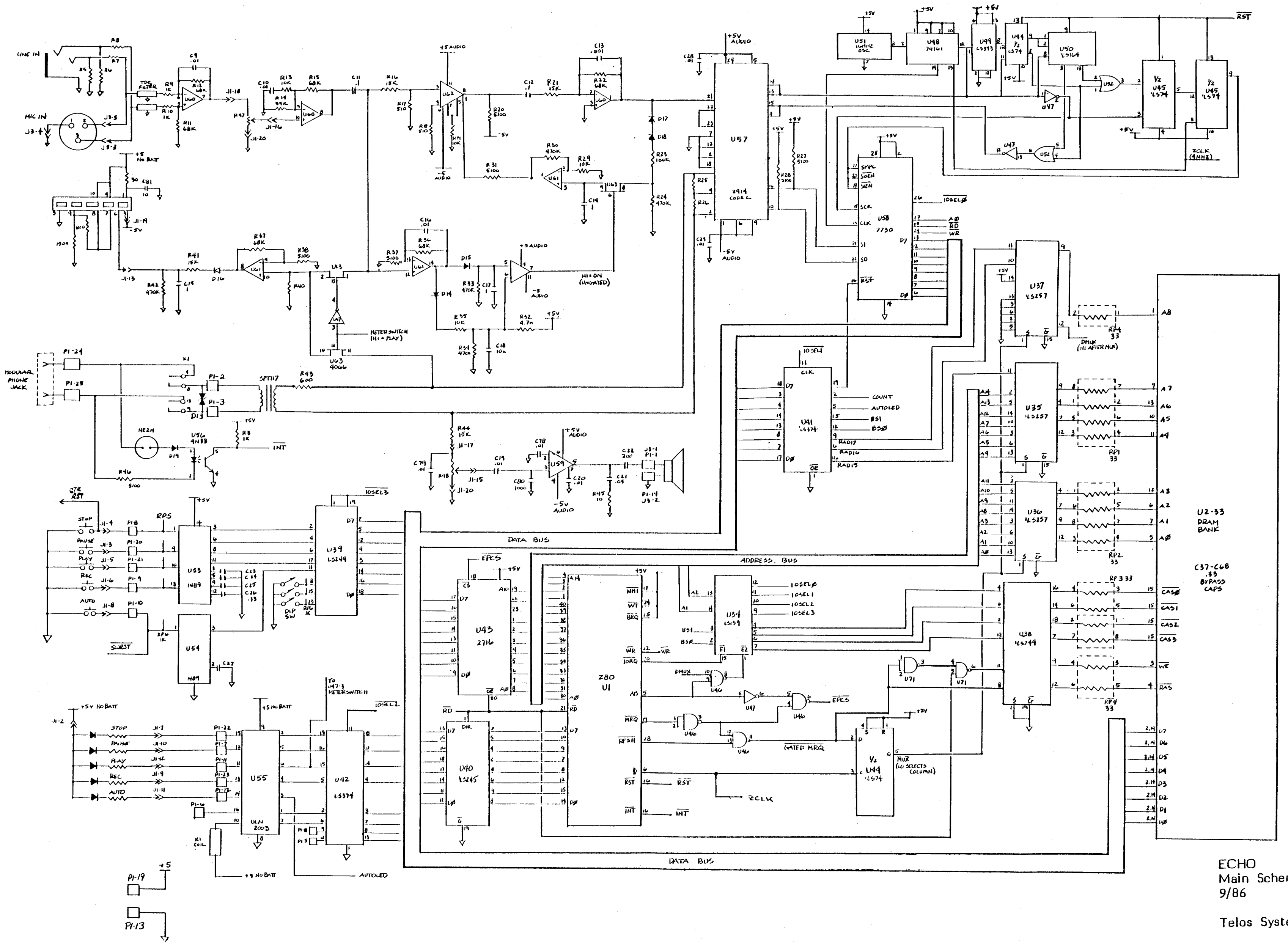






ECHO
Supplemental Schematic
9/86

Telos Systems



ECHO
Main Schematic
9/86

Telos Systems

PRELIMINARY

2913 AND 2914
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

- **2914 Asynchronous clocks, 8th bit signaling, loop back test capability**
- **2913 Synchronous clocks only, 300 mil package**

- **AT&T D3/D4 and CCITT Compatible**
- **Pin Selectable μ-law or A-law Operation**
- **Two Timing Modes:**
  - **—Fixed Data Rate Mode 1.536, 1.544, or 2.048 MHz**
  - **—Variable Data Rate Mode 64 kHz-4.096 MHz**
- **Exceptional Analog Performance**
- **Low Power HMOS-E Technology:**
  - **—5mW Typical Power Down**
  - **—140mW Typical Operating**
- **Fully Differential Architecture Enhances Noise Immunity**
- **On-Chip Auto Zero, Sample and Hold, and Precision Voltage References**
- **Direct Interface with Transformer or Electronic Hybrids**

The Intel 2913 and 2914 are fully integrated PCM codecs with transmit/receive filters fabricated in a highly reliable and proven N-channel HMOS silicon gate technology. These devices provide the functions that were formerly provided by two complex chips (2910A or 2911A and 2912A). Besides the higher level of integration, the performance of the 2913 and 2914 is superior to that of the separate devices.

The primary applications for the 2913 and 2914 are in telephone systems:

- Switching—Digital PBX's and Central Office Switching Systems
- Transmission—D3/D4 Type Channel Banks and Subscriber Carrier Systems
- Subscriber Instruments—Digital Handsets and Office Workstations

The wide dynamic range of the 2913 and 2914 (78 dB) and the minimal conversion time make them ideal products for other applications such as:

- Voice Store and Forward
- Digital Echo Cancellers
- Secure Communications Systems
- Satellite Earth Stations

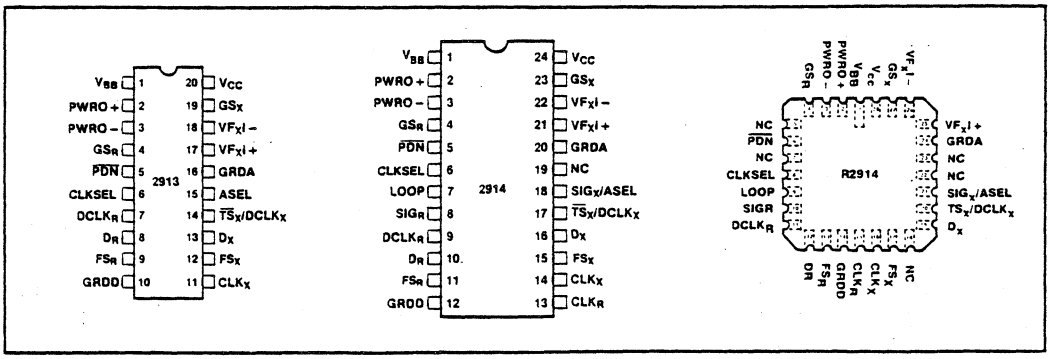


Figure 1. Pin Configurations

September 1983
Order Number 210629-002

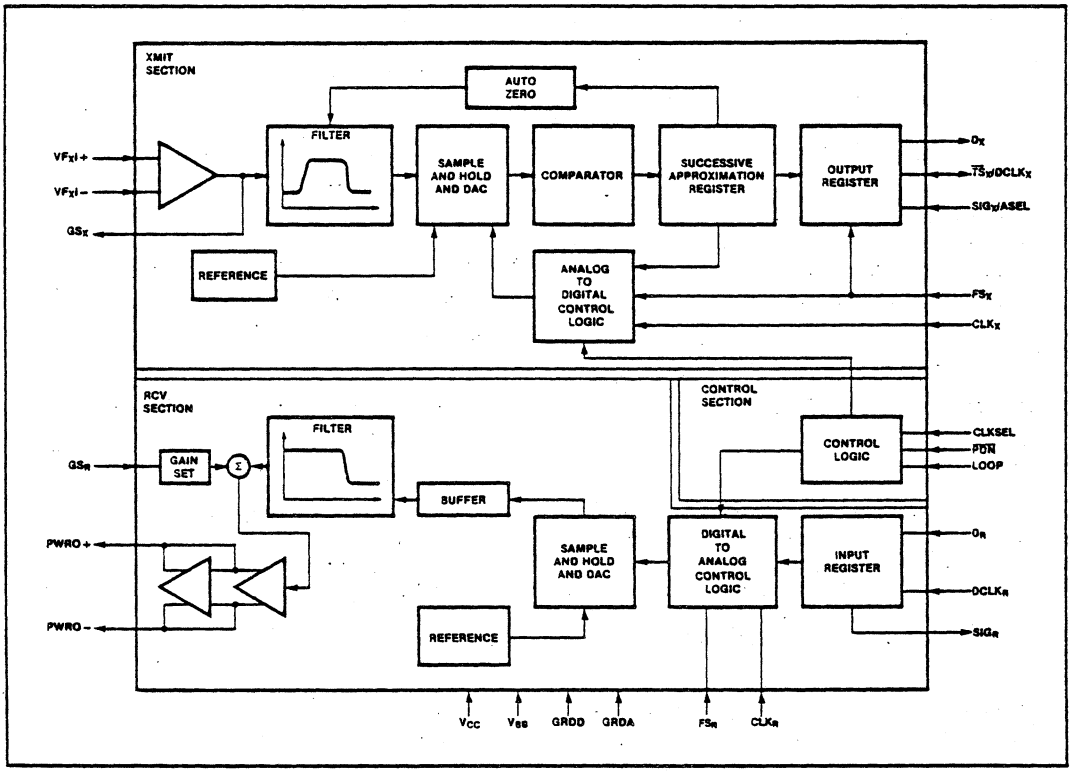


Figure 2. Block Diagram

Table 1. Pin Names

V_{BB}	Power (-5V)	GS_X	Transmit Gain Control
PWRO+, PWRO-	Power Amplifier Outputs	VF_XI-, VF_XI+	Analog Inputs
GS_R	Receive Gain Control	GRDA	Analog Ground
$\overline{PDN}$	Power Down Select	NC	No Connect
CLKSEL	Master Clock Frequency Select	SIG_X	Transmit Signaling Input
LOOP	Analog Loop Back	ASEL	μ- or A-law Select
SIG_R	Receive Signaling Bit Output	$\overline{TS_X}$	Timeslot Strobe/Buffer Enable
$DCLK_R$	Receive Variable Data Clock	$DCLK_X$	Transmit Variable Data Clock
D_R	Receive PCM Input	D_X	Transmit PCM Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+5V)	CLK_R	Receive Master Clock

Table 2. Pin Description

Symbol	Function
V_{BB}	Most negative supply; input voltage is -5 volts ±5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO-	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the gain setting network on the output power amplifier. Transmission level can be adjusted over a 12dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power down select. When $\overline{PDN}$ is TTL high, the device is active. When low, the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} ..... 2.048 MHz CLKSEL = GRDD ..... 1.544 MHz CLKSEL = V_{CC} ..... 1.536 MHz
LOOP	Analog loopback. When this pin is TTL high, the analog output (PWRO+) is internally connected to the analog input (VF_XI+), GS_R is internally connected to PWRO-, and VF_XI- is internally connected to GS_X. A 0dBm0 digital signal input at D_R is returned as a +3dBm0 digital signal output at D_X.
SIG_R	Signaling bit output, receive channel. In fixed data rate mode, SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. In this mode, the device is fully compatible with Intel 2910A and 2911A direct mode timing. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock which operates at TTL levels from 64kB to 4.096 MB data rates.
D_R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK_R in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8KHz frame synchronization clock input/ timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 300 milliseconds.

Symbol	Function
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
FS_X	8 KHz frame synchronization clock input/ timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 300 milliseconds.
D_X	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock: CLK_X in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer as in 2910A and 2911A direct mode timing. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 4.096 MB data rates.
SIG_X/ASEL	A dual purpose pin. When connected to V_{BB}, A-law operation is selected. When it is not connected to V_{BB} this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead.
NC	No connect
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI+	Non-inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply; input voltage is +5 volts ±5%.

FUNCTIONAL DESCRIPTION

The 2913 and 2914 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line or trunk.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

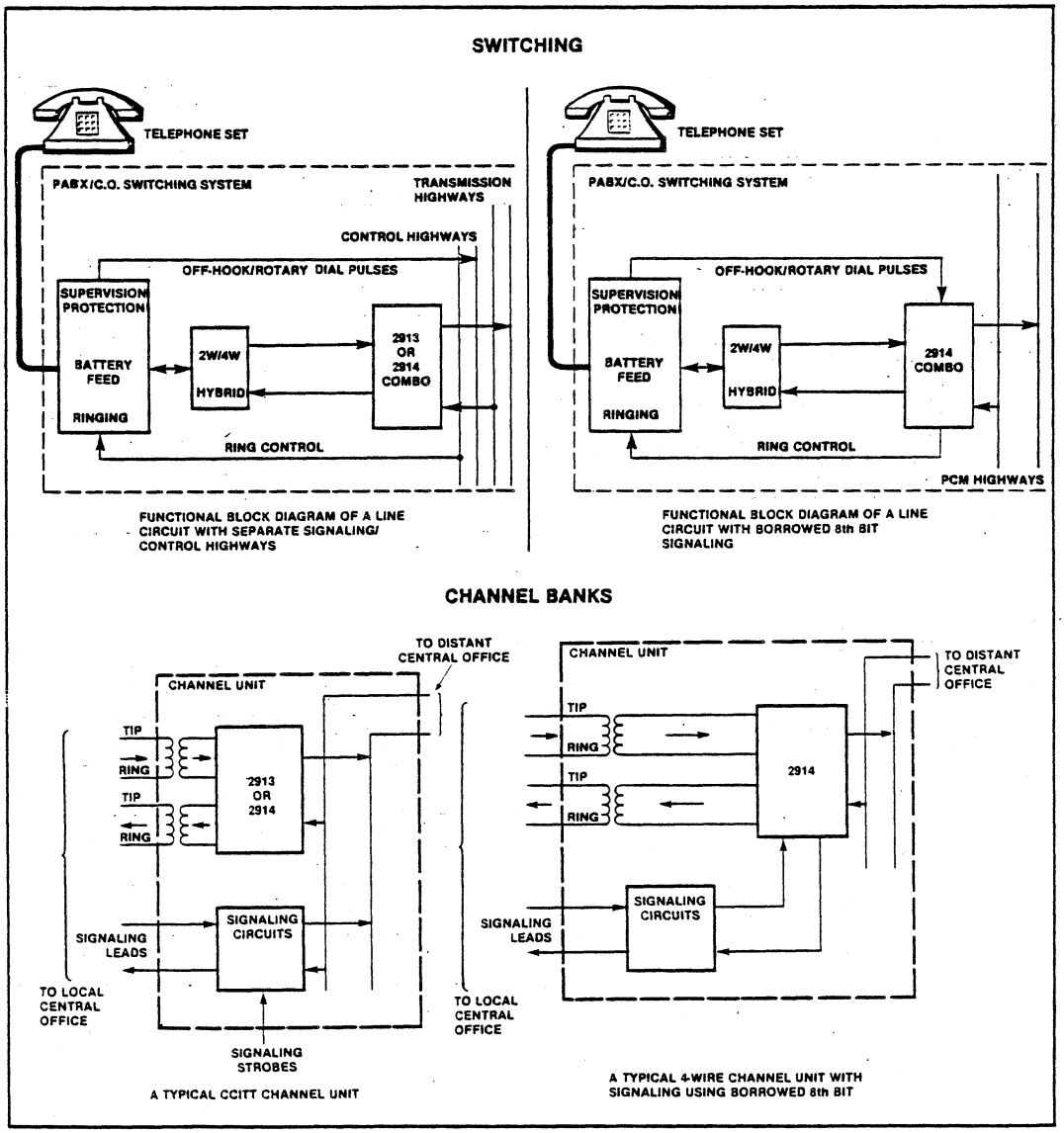
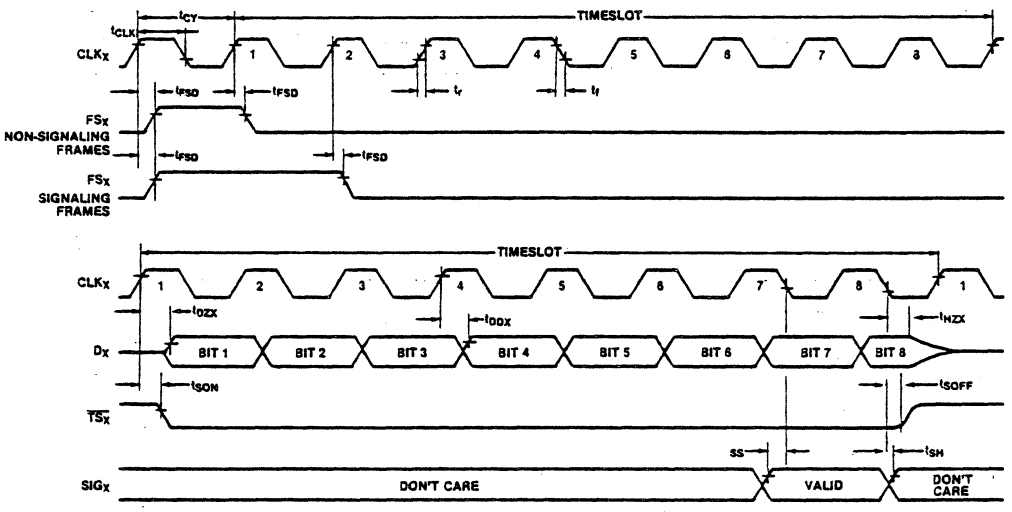


Figure 3. Typical Line Terminations

WAVEFORMS

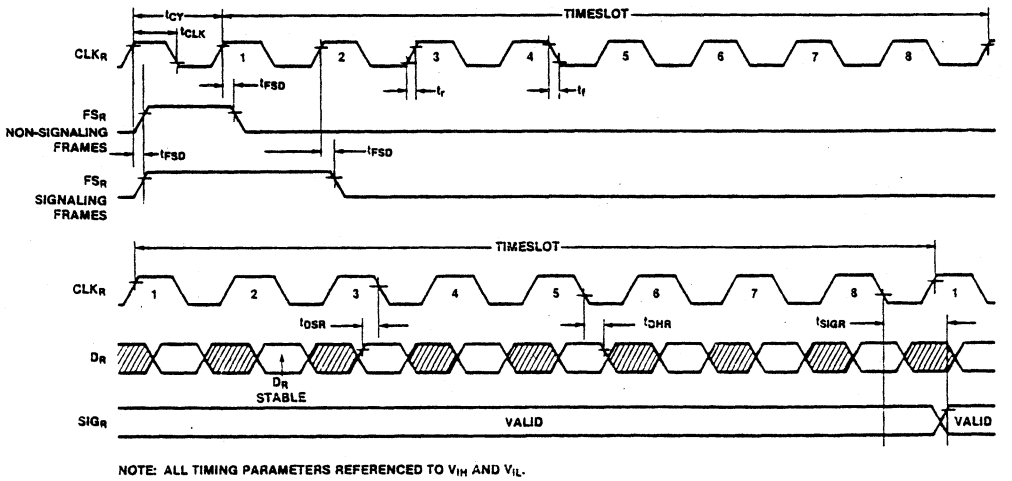
Fixed Data Rate Timing

TRANSMIT TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DZX}, t_{SOFF} AND t_{HZX} WHICH REFERENCE A HIGH IMPEDANCE STATE

RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL}.

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDX}	Timeslot Delay from $DCLK_X$	−80		80	ns	
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{DDX}	Data Delay from $DCLK_X$	0		100	ns	$0 < C_{LOAD} < 100$ pf
t_{DON}	Timeslot to D_X Active	0		50	ns	$0 < C_{LOAD} < 100$ pf
t_{DOFF}	Timeslot to D_X Inactive	0		80	ns	$0 < C_{LOAD} < 100$ pf
f_{DX}	Data Clock Frequency	64		2048[2]	kHz	
t_{DFSX}	Data Delay from FS_x	0		140	ns	t_{TSDX} = 80 ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDR}	Timeslot Delay from $DCLK_R$	−80		80	ns	
t_{FSD}	Frame Sync Delay	0		120	ns	
t_{DSR}	Data Setup Time	10			ns	
t_{DHR}	Data Hold Time	60			ns	
f_{DR}	Data Clock Frequency	64		2048[2]	kHz	
t_{SER}	Timeslot End Receive Time	0			ns	

64 KB OPERATION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{FSLX}	Transmit Frame Sync Minimum Downtime	488			ns	FS_X is TTL high for remainder of frame
t_{FSLR}	Receive Frame Sync Minimum Downtime	1952			ns	FS_R is TTL high for remainder of frame
t_{DCLK}	Data Clock Pulse Width			10	µs	

NOTES:

1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. Devices are available which operate at data rates up to 4.096 MHz.

51C256L
LOW POWER 256K X 1
CHMOS DYNAMIC RAM

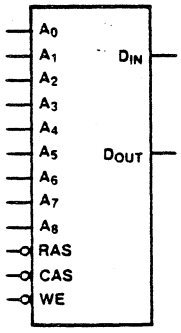
	51C256L-15	51C256L-20
Maximum Access Time (ns)	150	200
Maximum CHMOS Standby Current (mA)	0.1	0.1

- **Low Power Data Retention**
  - Standby current, CHMOS — 100 μA (max.)
  - Refresh period, $\overline{RAS}$-Only — 32 ms (max)
  - Data Retention Current — 230 μA (max.)
- **Low Operating Current — 65 mA (max.)**
- **TTL and HCT Compatible**
- **Low Input/Output Capacitance**
- **High Reliability Plastic — 16 Pin DIP**

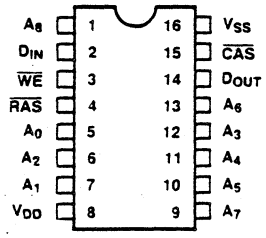
Intel® 51C256L is a low power 262,144 X 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C256L offers features not provided by an NMOS dynamic RAM: CHMOS standby current and extended $\overline{RAS}$-Only refresh for low data retention power. All inputs and outputs are TTL and HCT compatible and the input and output capacitances are significantly lowered to allow increased system performance.

The 51C256L offers a maximum standby current of 100 μA when $\overline{RAS} > V_{DD} - 0.5V$. During standby (i.e. refresh only cycles), the refresh period can be extended to 32 ms to reduce the total current required for data retention to less than 230 μA (max). The 51C256L combines this low power with high density for portable and battery backup applications.

LOGIC SYMBOL



PIN CONFIGURATION



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_8	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

June, 1984
Order Number: 280031-001

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under
Bias . . . . . −10°C to +80°C
Storage Temperature . . . Plastic −55°C to +125°C
Voltage on Any Pin except V_{DD} and D_{OUT}
Relative to V_{SS} . . . . . −2.0V to 7.5V
Voltage on V_{DD} Relative to V_{SS} . . . . −1.0V to 7.5V
Voltage on D_{OUT}
Relative to V_{SS} . . . . . −2.0V to V_{DD} +1V
Data Out Current . . . . . 50 mA
Power Dissipation 1.0W

†COMMENT:
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1]

$T_A = 0°C$ to 70°C, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	51C256L			Unit	Test Conditions	Notes
		Min.	Typ.[2]	Max.			
I_{DD1}	V_{DD} Supply Current, Operating		48	65	mA	$t_{RC} = t_{RC}$ (min), for −15 specification	3,4
			35	50	mA	$t_{RC} = t_{RC}$ (min), for −20 specification	
I_{DD2}	V_{DD} Supply Current, TTL Standby		1	2	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, all other inputs and output $\geq V_{SS}$	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh		45	65	mA	$t_{RC} = t_{RC}$ (min), for −15 specification	4
			35	50	mA	$t_{RC} = t_{RC}$ (min), for −20 specification	
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		3	4	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs and output $\geq V_{SS}$	3
I_{DD6}	V_{DD} Supply Current, CHMOS Standby		0.01	0.1	mA	$\overline{RAS} \geq V_{DD} - 0.5V$ and $\overline{CAS}$ at V_{IH}, all other inputs and output $\geq V_{SS}$	
$\lvert I_{LI} \rvert$	Input Load Current (any pin)			1	μA	$V_{IN} = V_{SS}$ to V_{DD}	
$\lvert I_{LO} \rvert$	Output Leakage Current for High Impedance State			10	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, $D_{OUT} = V_{SS}$ to V_{DD}	
V_{IL}	Input Low Voltage (all inputs)	−1.0		0.8	V		5
V_{IH}	Input High Voltage (all inputs)	2.4		$V_{DD}+1$	V		5
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 4.2$ mA	6
				0.1	V	$I_{OL} = 100\mu A$††	
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -5$ mA	6
				$V_{DD}-.1$	V	$I_{OH} = -100\ \mu A$††	

NOTES: †† Available 1Q 1985
1. All voltages referenced to V_{SS}.
2. Typical values are at $T_A = 25°C$ and $V_{DD} = +5V$.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) $\geq V_{SS}$ and V_{IH} (max) $\leq V_{DD}$.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

†NOTE:
Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

A.C. CHARACTERISTICS[1,2,3]

$T_A = 0°c$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

#	JEDEC Symbol	Symbol	Parameter	51C256L-15		51C256L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	150	75000	200	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	245		315		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	85		105		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	150		200		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	30	75000	35	75000	ns	
6	t_{WH2RL2}	t_{WRP}	Write to $\overline{RAS}$ Precharge Time	10		10		ns	
7	t_{RL1WL2}	t_{RWH}	$\overline{RAS}$ to Write Hold Time	20		25		ns	
8	t_{AVRL}	t_{ASR}	Row Address Set-up Time	0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	20		25		ns	
10	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		ns	
11	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		ns	
12	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	35	120	40	165	ns	4
13	t_{AVCL2}	t_{ASC}	Column Address Set-up Time	5		5		ns	
14	t_{CL1AX}	t_{CAH}	Column Address Hold Time	20		25		ns	
15	t_{RL1AX}	t_{AR}	Column Address Hold Time From $\overline{RAS}$	70		80		ns	
	t_{RVRV}	t_{REF1}	Time Between Refresh		4		4	ms	5
	t_{RVRV}	t_{REF2}	Time Between Refresh ($\overline{RAS}$-Only)		32		32	ms	5
	t_T	t_T	Transition Time (Rise and Fall)	3	25	3	25	ns	6
16	t_{CL1QX}	t_{ON}	Output Buffer Turn On Delay	0	30	0	35	ns	
17	t_{CH2QZ}	t_{OFF}	Output Buffer Turn Off Delay	0	25	0	30	ns	

NOTES:
1. All voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).
3. A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF V_{IL} (min) $\geq V_{SS}$ and V_{IH} (max) $\leq V_{DD}$.
4. t_{RCD} (max) is specified for reference only.
5. The 51C256L extends the refresh period to 32 ms during $\overline{RAS}$-Only refresh operation.
6. t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. CHARACTERISTICS (Con't.)

Read Cycle

#	JEDEC Symbol	Symbol	Parameter	51C256L-15		51C256L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
18	t_{RL1QV}	t_{RAC}	Access Time From $\overline{RAS}$		150		200	ns	7
19	t_{CL1QV}	t_{CAC}	Access Time From $\overline{CAS}$		30		35	ns	8, 9
20	t_{AVQV}	t_{CAA}	Access Time From Column Address		70		90	ns	9
21	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		ns	
22	t_{WH2CL2}	t_{RCS}	Read Command Set-up Time	0		0		ns	
23	t_{AVRH1}	t_{CAR}	Column Address $\overline{RAS}$ Set-up Time	70		90		ns	
24	t_{CH2WX}	t_{RCH}	Read Com. Hold Time Referenced to $\overline{CAS}$	0		0		ns	10
25	t_{RH2WX}	t_{RRH}	Read Com. Hold Time Referenced to $\overline{RAS}$	10		10		ns	10

Write Cycle

#	JEDEC Symbol	Symbol	Parameter	51C256L-15		51C256L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	30		35		ns	
27	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		ns	
28	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35		ns	
29	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	25		30		ns	
30	t_{WL1CL2}	t_{WCS}	Write Command Set-up Time	0		0		ns	11
31	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	30		35		ns	
32	t_{DVCL2}	t_{DS}	Data-In Set-up Time	0		0		ns	
33	t_{CL1DX}	t_{DH}	Data-In Hold Time	25		30		ns	

NOTES:

7. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If $t_{RCD} \geq t_{RCD}$ (max), then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).
8. Assumes $t_{RCD} \geq t_{RCD}$ (max).
9. If $t_{ASC} < (t_{CAA}$ (max) $- t_{CAC}$ (max) $- t_T)$, then access time is defined by t_{CAA} rather than by t_{CAC}.
10. Either t_{RCH} or t_{RRH} must be satisfied.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (Con't.)

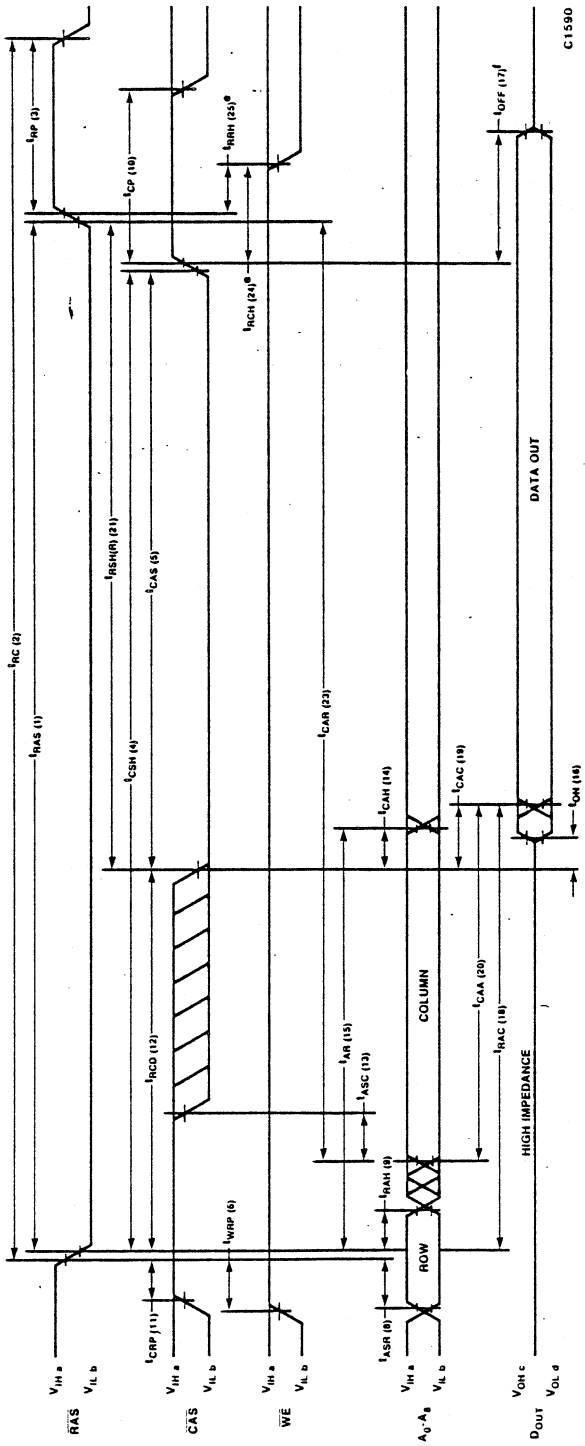
Read-Modify-Write- Cycle[12]

#	JEDEC Symbol	Symbol	Parameter	51C256L-15		51C256L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
34	$t_{RL2RL2(RMW)}$	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	280		355		ns	
35	$t_{RL1RH1(RMW)}$	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	185		240		ns	
36	$t_{CL1CH1(RMW)}$	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	65		75		ns	
37	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	150		200		ns	13
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	30		35		ns	13
39	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	70		90		ns	13

NOTES:

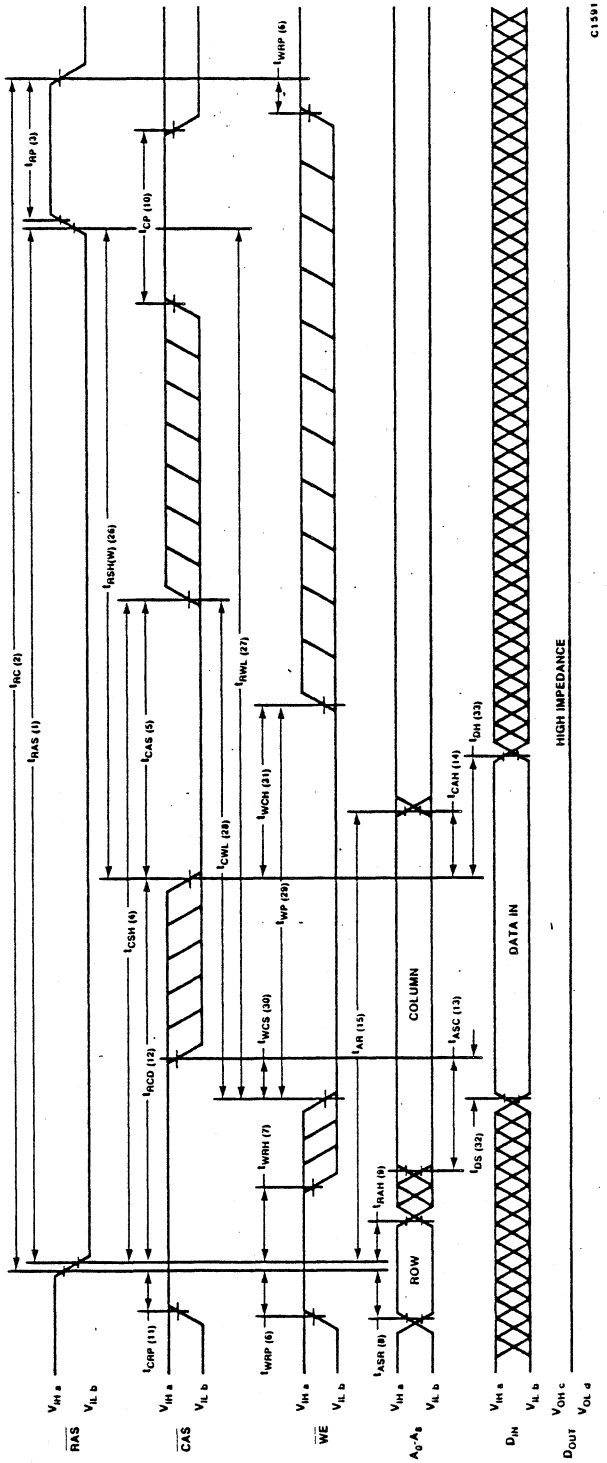
12. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.

WAVEFORMS
Read Cycle



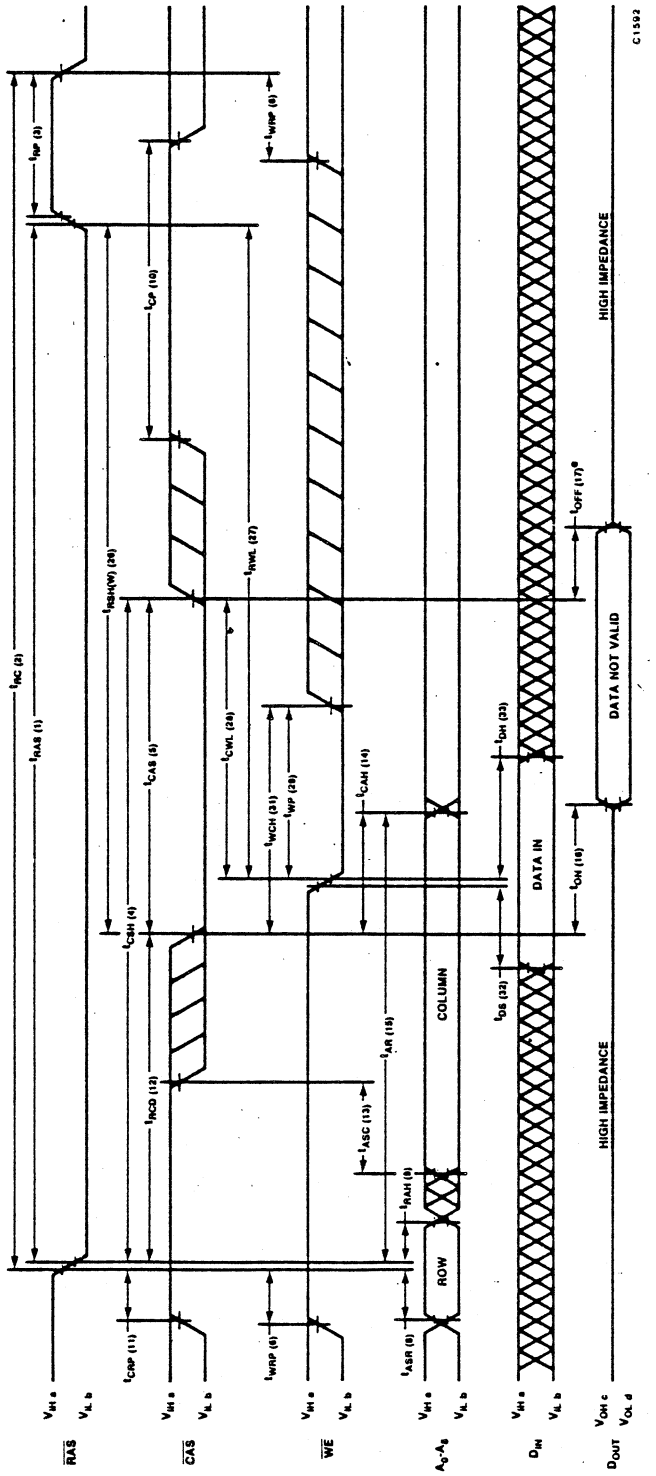
NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. Either t_{RCH} or t_{RPH} must be satisfied.
f. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.

WAVEFORMS (Cont.)
Write Cycle ($\overline{CAS}$ Controlled)[e]



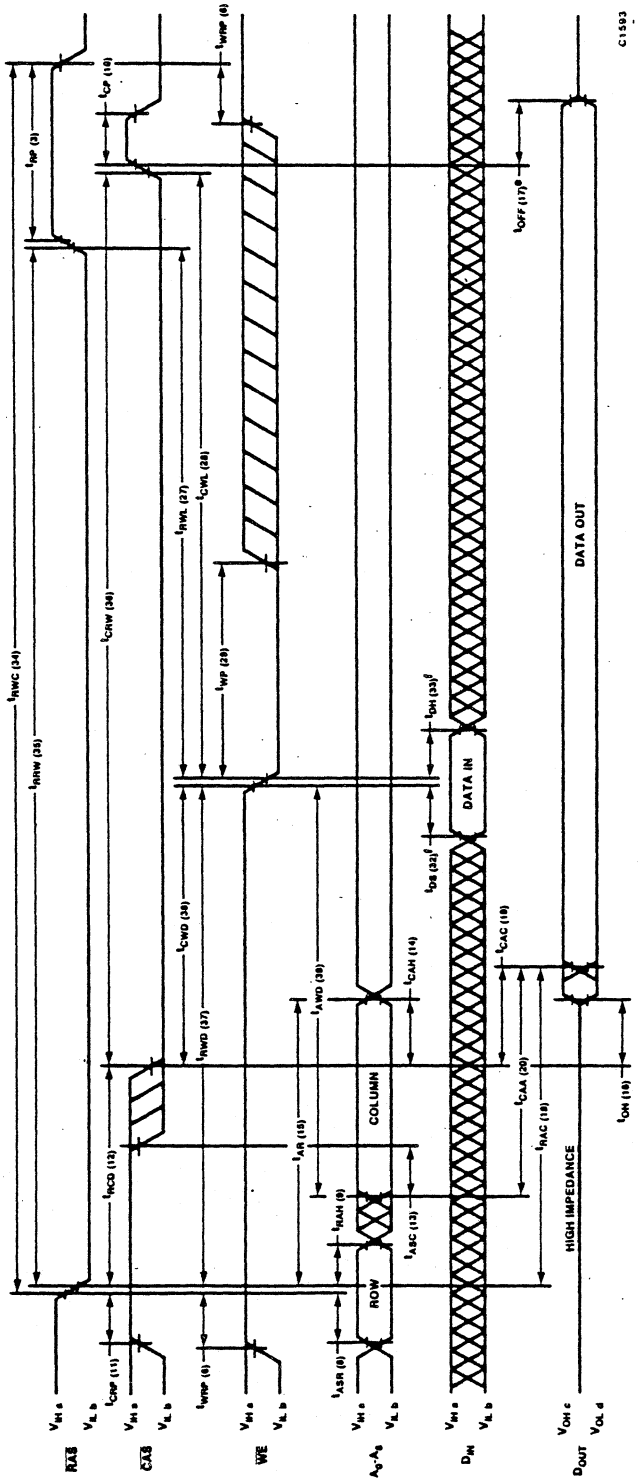
NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column address and data-in.

WAVEFORMS (Cont.)
Write Cycle ($\overline{WE}$ Controlled)[f]



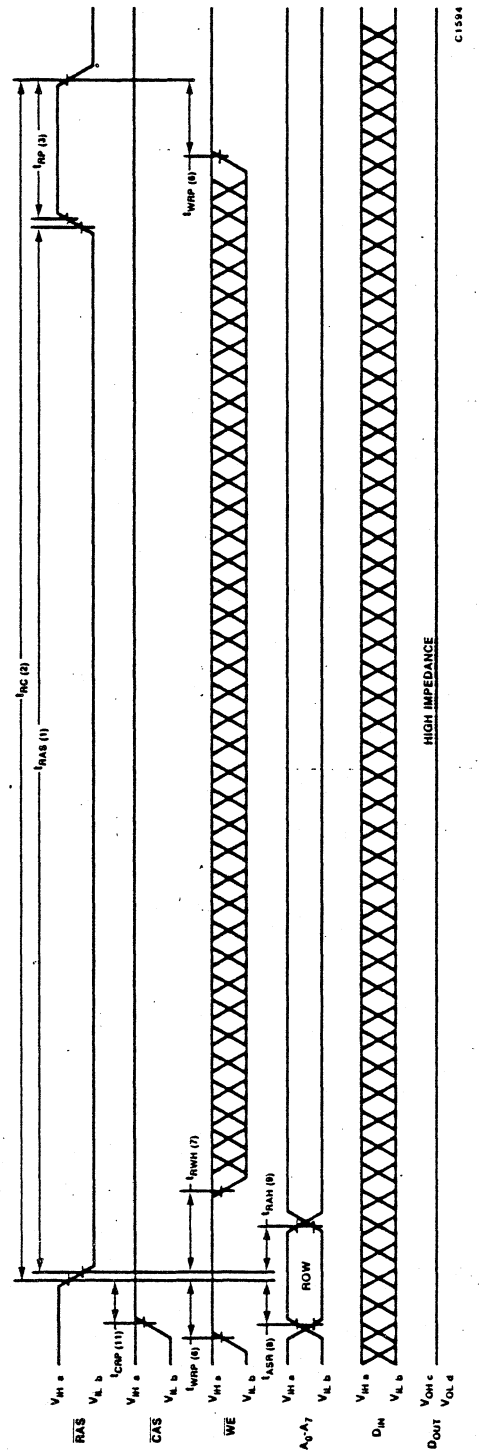
NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the data-in.

WAVEFORMS (Cont.)
Read/Modify/Write Cycle



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
f. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

WAVEFORMS (Cont.)
RAS-Only Refresh Cycle



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

FUNCTIONAL DESCRIPTIONS

The 51C256L is a CHMOS dynamic RAM optimized for low power applications. The functionality is similar to a traditional dynamic RAM. The 51C256L reads and writes data by multiplexing an 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP}, has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out becomes valid only when t_{RAC}, t_{CAA}, and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched in by $\overline{CAS}$. The write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the later of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ will maintain the output in the high impedance state; terminating with $\overline{WE}$ allows the output to go active.

The 51C256L incorporates a self-timed write feature which simplifies the system interface. The write function is internally timed on a write command which allows for a fast write pulse width and a fast write precharge time, thus eliminating the need for critical placement of transitions during the write cycle.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only cycle will perform refresh.

Extended Refresh Cycle

The 51C256L extends the refresh cycle period to 32 milliseconds for $\overline{RAS}$-Only refresh cycles. This feature reduces the total current consumption to a maximum of 230 micro Amperes, and typically 90 micro Amperes, for data retention ($\overline{RAS}$-Only refresh operation for the 51C256L-20). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC})(I_{Active}) + (t_{RI} - t_{RC})(I_{Standby})}{t_{RI}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time of $t_{REF}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

Data Out Operation

The 51C256L Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).

The V_{DD} current (I_{DD}) requirement of the 51C256L during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*, and A.P. #172, *CHMOS DRAMS in Graphics Applications*.

Table 1. Intel 51C256L Data Output Operation for Various Types of Cycles

Cycle	Data Out State
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Only Cycle	High Impedance

GLOBE gel/cell®

Two Types of GEL/CELL Batteries

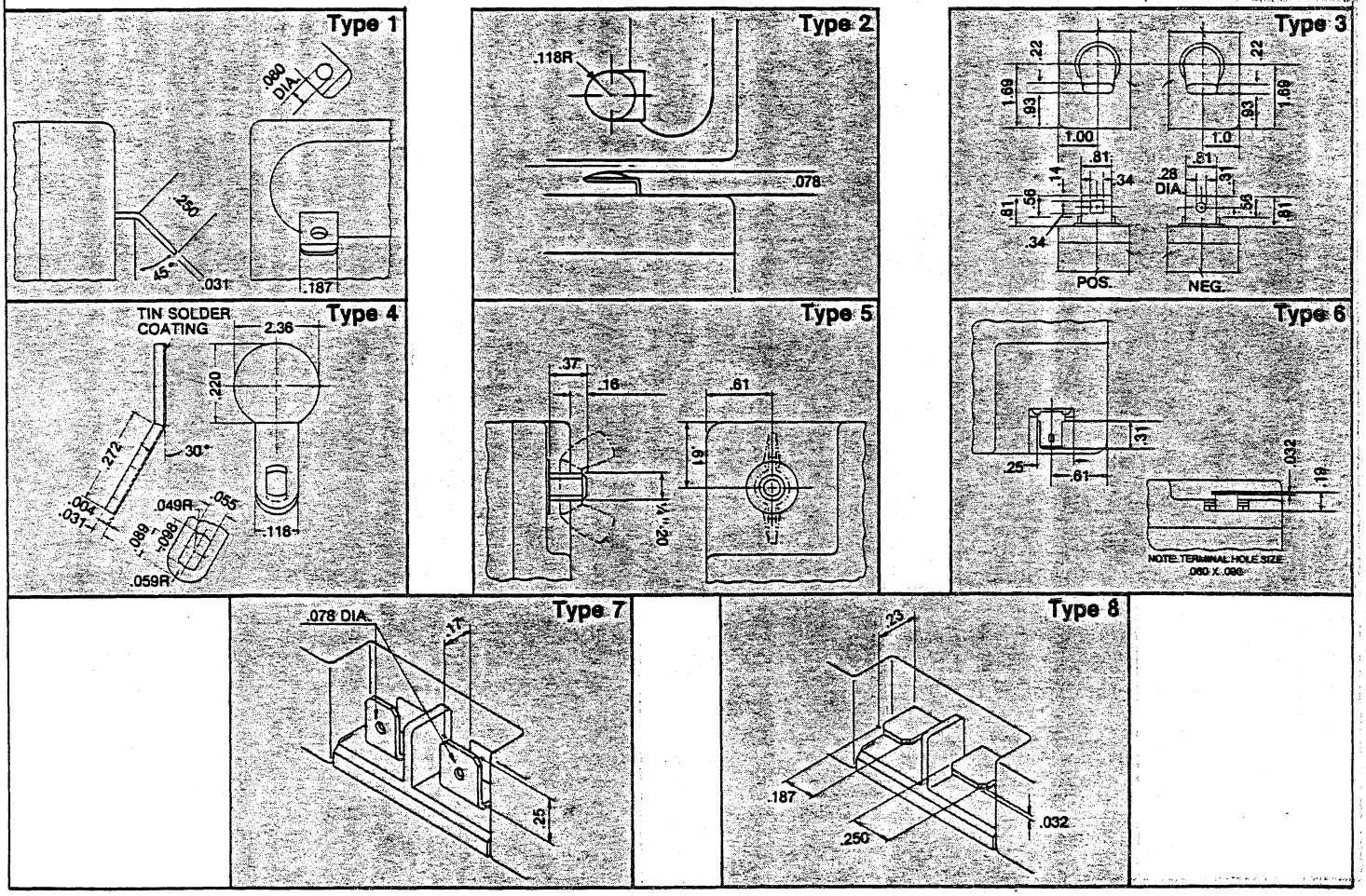
Gel/Cell Type "A" for Standby Power Use
Gel/Cell Type "B" for Frequent Cycle Use

To tailor the battery for the specific application, Globe offers the Gel/Cell in two distinct types.

	Type A	Type B
Initial Capacity	Typically 90-100%	Typically 80-90%
Cycle Life	100-150 Cycles to 50% Capacity	250-500 Cycles to 50% Capacity
Float Service Life	4-6 Years at 25°C (77°F)	3-5 Years at 25°C (77°F)
Float Current Acceptance (2.25V/cell)	0.5-1.5 ma/A.H. (@ 25°C)	1.0-5.0 ma/A.H. (@ 25°C)

Globe Part No.	Standard Terminal No.	Terminal Option No.
GC 410	-4	-
GC 610	-1	-
GC 1215	-1	-
GC 620	-1	-
GC 426	-1	-
GC 626	-1	-2
→ GC 826	-1	-
GC 645	-1	-
GC 1245	-1	-
GC 660	-1	-
GC 1260	-1	-
GC 665	-7	-8
GC 280	-1	-
GC 680	-1	-
GC 690	-7	-8
GC 6100	-7	-8
GC 6120	-7	-8
GC 6200	-5	-
GC 12230	-6	-5
U-128	-3	-
GC 12550	-3	-

Terminal Types



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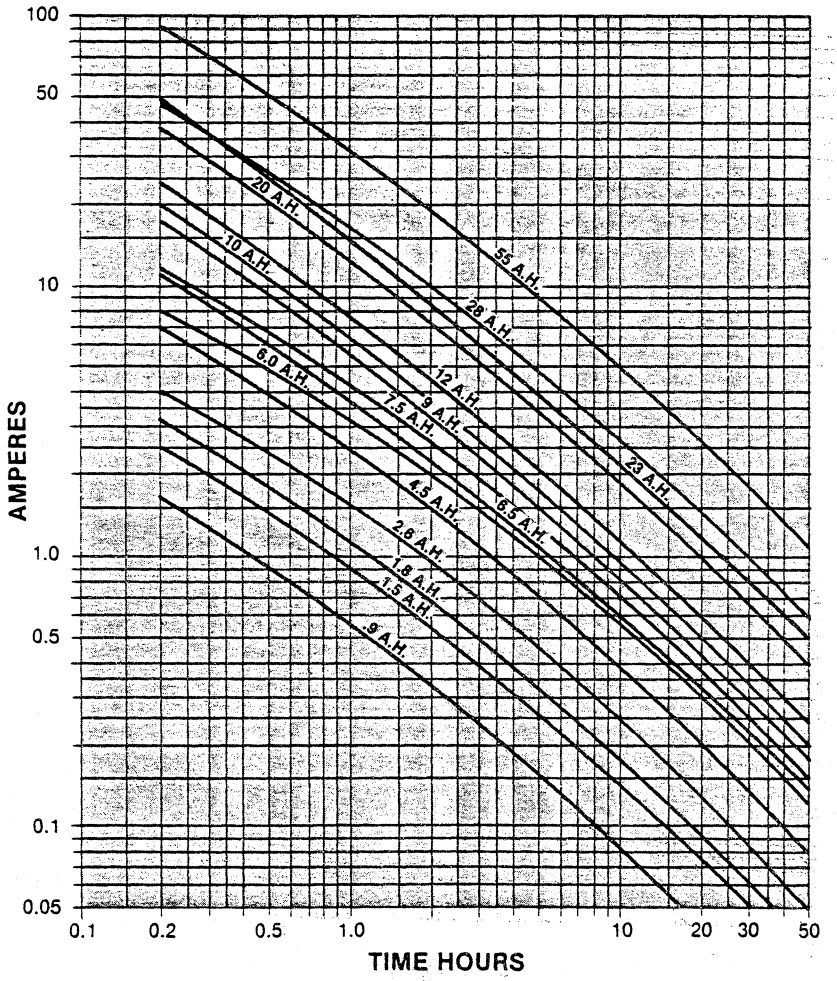
GEL/CELL Selection Chart

The chart shown below can be used to find the approximate size Gel/Cell battery required for a given operating time when the current drain is known.

To use the chart, locate the intersection of the operating time line with the horizontal line corresponding to current drain. The capacity line above this intersection corresponds to the ***approximate*** ampere-hour battery requirement.

Refer to the following discharge curves for more accurate operating time.



Telos Systems ECHO VOICE STORAGE/RETRIEVAL SYSTEM

Warranty and Application Caution

The Telos Echo is warranted to be free from defects in material and workmanship for a period of 120 days Written notice of claim must be received by seller within the warranty period In the event of a defect during the warranty period, if customer returns the defective part or the entire unit to a place designated by the seller transportation prepaid, seller will at it's option either repair or replace the part or the unit, and such action by seller shall be the full extent of the seller's obligation Seller will pay the transportation charges to return the part or unit to the customer The warranty is void if the unit is subject to misuse, accident, neglect, or damage

No other warranties, express or implied, all of which are specifically excluded, including, but not limited to the warranties of merchantability of fitness for a particular purpose, shall be applicable to any equipment sold hereunder, and the foregoing shall constitute the customer's sole right and remedy In no event shall the seller or it's agents be liable for incidental or consequential damages, or for loss, damage, or expense directly or indirectly arising from use of the product, or any inability to use them either separate or in combination with other equipment or materials, or from any other cause.

Depending on the application, equipment may require an FCC registered protective interface. The user is responsible to provide such, if required.